Docket No.: SON-3058
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Masaki Murase et al.

Application No.: 10/564,473 | Confirmation No.: 9263

Filed: January 13, 2006 | Art Unit: 2629

For: DELAY TIME CORRECTION CIRCUIT, VIDEO DATA PROCESSING CIRCUIT, AND FLAT DISPLAY DEVICE | Examiner: G. Sitta

REPLY BRIEF

MS Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

INTRODUCTORY COMMENTS

This is a Reply Brief under 37 C.F.R. §41.41 in response to the Examiner's Answer dated March 30, 2010.

Regarding any new issue raised in the Reply Brief, if present, U.S. patent practice and procedures set forth within 37 C.F.R. §41.43(a)(1) instructs as follows:

> After receipt of a reply brief in compliance with § 41.41, the primary examiner must acknowledge receipt and entry of the reply brief. In addition, the primary examiner may withdraw the final rejection and reopen prosecution or may furnish a supplemental examiner's answer responding to any new issue raised in the reply brief.

All arguments presented within the Appeal Brief of February 12, 2010 are incorporated herein by reference.

Additional **Remarks/Arguments** begin on page 3 of this paper.

REMARKS

i. Standards of review.

The Patent and Trademark Office has the burden of showing a prima facie case of obviousness. *In re Bell*, 26 USPQ2d 1529, 1530 (Fed. Cir. 1993).

The Patent and Trademark Office ***may not***, because it may doubt that the invention is patentable, resort to speculation, unfounded assumptions or hindsight reconstruction to supply deficiencies in its factual basis. *In re Warner and Warner*, 154 USPQ 173, 178 (C.C.P.A. 1967).

In determining the propriety of the Patent and Trademark Office case for prima facie obviousness, it is necessary to ascertain whether the prior art teachings would appear to be sufficient to one of ordinary skill in the art to suggest making the proposed substitution or other modification. *In re Taborsky*, 183 USPQ 50, 55 (CCPA 1974).

The mere fact that the prior art could be so *modified* ***would not*** have made the modification obvious unless the prior art suggested the desirability of the modification. *In re Gordon*, 221 USPQ 1125, 1127 (Fed. Cir. 1984).

There is no suggestion to combine if a reference ***teaches away*** from its combination with another source. *Tec Air, Inc. v. Denso Mfg. Mich. Inc.*, 52 USPQ2d 1294, 1298 (Fed. Cir. 1999).

A reference may be said to teach away when a person of ordinary skill, upon reading the reference, ***would be discouraged*** from following the path set out in the reference, or would be led in a ***direction divergent*** from the path that was taken by the applicant. *In re Gurley*, 31 USPQ2d 1130, 1131 (Fed. Cir. 1994).

If references taken in combination would produce a "***seemingly inoperative device***," such references ***teach away*** from the combination and thus ***cannot serve as predicates*** for a prima facie case of obviousness. *McGinley v. Franklin Sports Inc.*, 60 USPQ2d 1001, 1010 (Fed. Cir. 2001).

i. The Examiner erred in rejecting claims 7-21 as allegedly being unpatentable over the "Background Art" of the specification for the present application (AAPA) in view of Japanese Application Publication No. 2002-009594 (Iemoto).

A. Claims 7-11, 13-17, 19-21 stand or fall together.

Claims 8-11, 13-17, 19-21 are dependent upon claim 7. Claim 7 is drawn to a display device comprising:

> a level shifter (1) configured to change an amplitude of gradation data (D1) from a first voltage range to a second voltage range, amplified gradation data being said gradation data (D1) at said second voltage range,
>
> wherein output data (D2) during a quiescent period (T2) is dummy data (DD), said output data (D2) during a period (T1) other than said quiescent period (T2) being said amplified gradation data.

For convenience, Figure 5 of the specification for the instant application is provided hereinbelow.

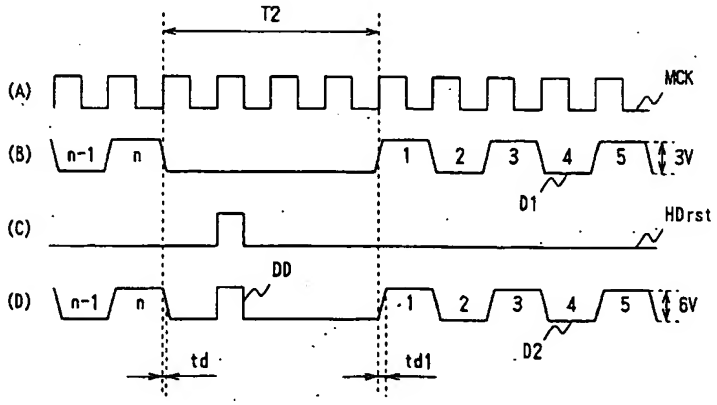


Fig.5

1. "Background Art" of the specification for the present application (AAPA) *fails* to disclose teach, or suggest *output data during a quiescent period being dummy data.*

Figure 2 of AAPA is provided hereinbelow.

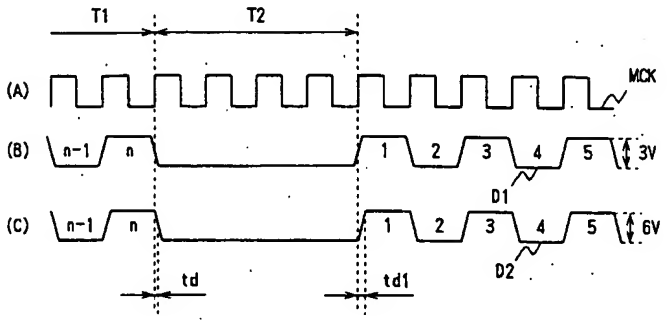


Fig.2

Page 9 of the Examiner's Answer ***concedes*** that AAPA ***fails*** to teach output data during a quiescent period (T2) being dummy data.

Thus, the Examiner's Answer ***fails*** to show that AAPA, alone, discloses *output data during a quiescent period being dummy data.*

2. Japanese Application Publication No. 2002-009594 (Iemoto) *fails* to disclose teach, or suggest *output data during a quiescent period being dummy data.*

As an initial matter, the Examiner's Answer ***fails*** to identify a quiescent period within Iemoto. Instead, pages 10-11 of the Examiner's Answer merely assert that:

> *Therefore, Examiner respectfully disagrees with Applicant contentions that Iemoto fails to teach wherein output data during a quiescent period is dummy data because*

dummy pulse generating means (30) outputs a dummy pulse when the present signal is not the "target signal", or quiescent period.

In response, Figures 1 and 2 of Iemoto are provided hereinbelow.

Figure 1 of Iemoto

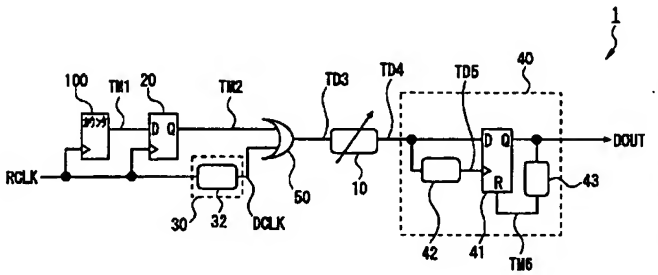
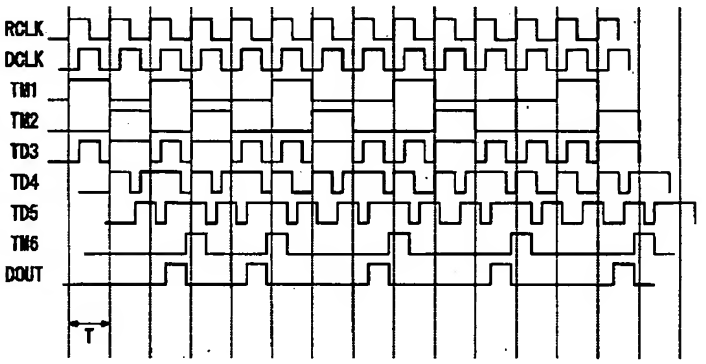


Figure 2 of Iemoto



The page 11 of the Examiner's Answer refers to the *"target signal", or quiescent period* in the alternative.

Being presented in the alternative, a clear definition of "*quiescent period*" within Iemoto has not been articulated within the Examiner's Answer, thereby leaving such a definition as mere speculation.

Moreover, paragraph [0012] of Iemoto arguably discloses that a dummy pulse creating means (for example, dummy pulse generating circuit 30 shown in drawing 1) which generates a dummy pulse signal of different pulse width from a cycle of this reference signal based on said input pulse signal or said reference signal.

In this regard, Figure 1 of Iemoto arguably depicts an OR gate 50, with DCLK and TM2 being inputs and TD3 being an output.

For example, the cycle for the time delay of the request set up beforehand is calculated, and the counter 100 delays it from the count start signal which does not illustrate the inputted reference signal RCLK, and is ***outputted as signal TM1*** (Iemoto at paragraph [0022]).

The flip-flop 20 makes data *input signal TM1* inputted from the counter 100, and ***outputs signal TM2*** which held signal TM1 by the rising edge to OR gate 50 by making into a clock pulse signal the reference signal RCLK which is the constant period T (Iemoto at paragraph [0023]).

The delay circuit 32 is larger than the time delay of the flip-flop 20, and delays the inputted reference signal RCLK within the time of the cycle T and the difference of pulse width of the reference signal RCLK, and *outputs* ***delay clock signal DCLK*** *to OR gate 50 as a* ***dummy pulse signal*** (Iemoto at paragraph [0024]).

Paragraph [0025] of Iemoto arguably discloses that OR gate 50 carries out OR operation of the delay clock signal DCLK inputted as signal TM2 inputted from the flip-flop 20 from the delay circuit 32, and outputs it to the vernier 10 as ***mix-signals TD3***.

However, the Examiner's Answer ***fails*** to describe TM2 as being "*output data*".

In particular, the Examiner's Answer ***fails*** *to show TM2* during a period other than a quiescent period ***being amplified gradation data***, especially when the amplified gradation data is *gradation data at a second voltage range*.

This deficiency has been highlighted within the Appeal Brief at page 9.

Likewise, the Examiner's Answer ***fails*** to show the ***mix-signals TD3*** as including amplified gradation data.

Instead of refuting these observations regarding the failure of Iemoto in disclosing the claimed features, page 11 of the Examiner's Answer only refers to AAPA, contending that:

However, Examiner is relying on AAPA to teach wherein the amplified gradation data being gradation data at a second voltage range, as can be seen in fig. 2 of AAPA, (c) is outputted at 6v which is amplified from 3v.

Thus, the Examiner's Answer ***fails*** to show that Iemoto, alone, discloses *output data during a quiescent period being dummy data.*

3. Combination of "Background Art" of the specification for the present application (AAPA) and Japanese Application Publication No. 2002-009594 (Iemoto).

The Examiner's Answer has relied upon the combination of AAPA and Iemoto.

However, a comparison of AAPA and Iemoto reveals that the skilled artisan would not have referred to the disclosure of Iemoto for the purpose of modifying AAPA.

Figure 1 of AAPA and Figure 1 of Iemoto are provided hereinbelow.

Figure 1 of AAPA

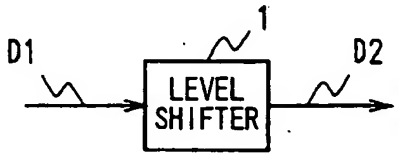


Figure 1 of Iemoto

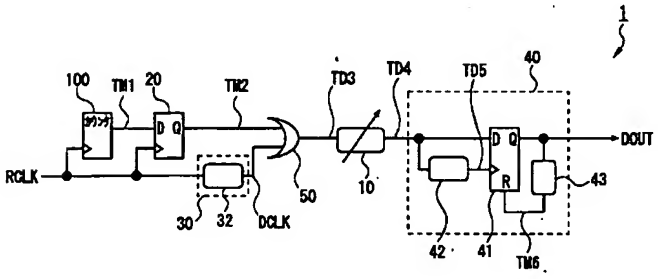


Figure 2 of AAPA and Figure 2 of Iemoto are provided hereinbelow.

Figure 2 of AAPA

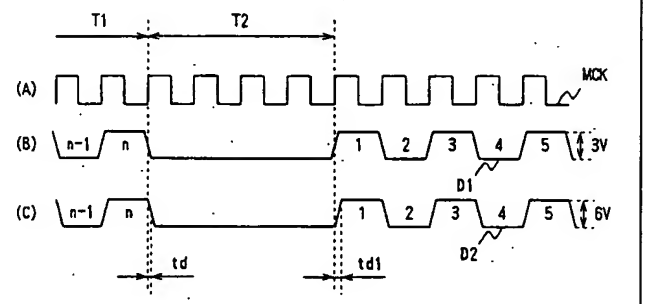
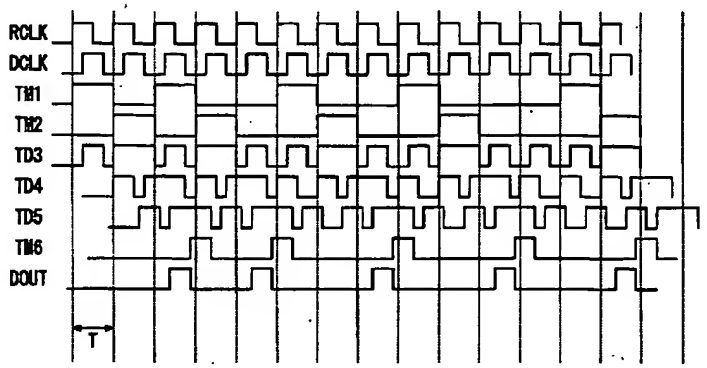


Figure 2 of Iemoto



a) The level shifter of claim 7.

Claim 7 on appeal includes *a level shifter (1) configured to change an* ***amplitude of gradation data (D1)*** *from a first voltage range to a second voltage range,* ***amplified gradation data*** *being said gradation data (D1) at said second voltage range.*

b) The output data of claim 7.

Within claim 7, *output data (D2) during a quiescent period (T2) is dummy data (DD), said output data (D2) during a period (T1) other than said quiescent period (T2) being* ***said amplified gradation data***.

c) The Examiner's Answer *fails* to show that input data D1 of AAPA and TM2 of Iemoto are suitable for substitution.

Paragraph [0009] of AAPA provides that more specifically, in this kind of logical circuit, as shown in FIGS. 1 and 2, for example, if ***input data D1 (FIG. 2(B)) synchronized with a main clock MCK (FIG. 2(A))*** is inputted to a level shifter 1 so as to output the input data D1 with an amplitude of 0 to 3 (V) converted to 0 to 6 (V), during a period T1 in which the logical level of the gradation data D1 switches at a duty ratio of 50 (%), a delay time tD is approximately constant.

Paragraph [0023] of Iemoto provides that the flip-flop 20 makes data *input signal TM1* inputted from the counter 100, and ***outputs signal TM2*** which held signal TM1 by the rising edge to OR gate 50 by making into a ***clock pulse signal the reference signal RCLK*** which is the constant period T.

However, the Examiner's Answer ***fails*** to show that *input data D1* of AAPA and *TM2* of Iemoto are one in the same.

For example, Iemoto ***fails*** to disclose any circuitry within Figure 1 that is remotely capable of changing an amplitude of TM2 from a first voltage range to a second voltage range.

Instead, Figure 1 of Iemoto shows the output of flip-flop 20 being fed directly into the OR gate 50 without the presence of an intervening level shifter.

Moreover, the Examiner's Answer ***fails*** to show that the skilled artisan would have inserted the level shifter 1 of AAPA between the flip-flop 20 and OR gate 50 of Iemoto.

Thus, the Examiner's Answer ***fails*** to show that the combination of AAPA and Iemoto discloses *output data during a quiescent period being dummy data.*

d) The Examiner's Answer *fails* to show that output data D2 of AAPA and TM2 of Iemoto are suitable for substitution.

Paragraph [0010] of AAPA provides that accordingly, as shown in FIG. 3, in the case where each *bit D1 (FIGS. 3(B1) and 3(B2)) of the gradation data is* ***level-shifted*** and is latched by a subclock SCK (FIG. 3(A)) if the gradation data is data supplied at a high transfer speed, ***output data D2A*** of the level shifter 1 can be correctly latched by the subclock SCK (FIGS. 3(B1) and 3(C1)) during the period T1 in which the logical level of each bit D1 of the gradation data switches at the duty ratio of 50 (%), but immediately after a vertical blanking period VBL, for example, the ***output data D2*** of the level shifter 1 cannot be correctly latched (FIGS. 3(B2) and 3(C2)).

Here, Figure 2 of Iemoto ***fails*** to disclose TM2 being level-shifted.

Figure 2 of Iemoto ***fails*** to disclose TM2 being latched by either RCLK or DCLK.

Whereas AAPA provides that each bit D1 (FIGS. 3(B1) and 3(B2)) of the gradation data is *level-shifted* and is *latched by a subclock SCK* (FIG. 3(A)), Iemoto ***fails*** to disclose TM2 as having the capability of being either level-shifted and being latched by either RCLK or DCLK.

Likewise, Figure 1 of AAPA ***fails*** to show an OR gate or any other circuitry that receives output data (D2).

Whereas AAPA provides that output data D2A of the level shifter 1 can be correctly *latched by the subclock SCK* (FIGS. 3(B1) and 3(C1)), Iemoto ***fails*** to disclose TM2 as having the capability of being *latched by either RCLK or DCLK.*

Thus, the Examiner's Answer ***fails*** to show that *output data during a quiescent period being dummy data* would have been obvious as a result of the combination of AAPA and Iemoto.

e) The combination of AAPA and Iemoto as proposed within the Examiner's Answer would produce a "*seemingly inoperative device*".

Page 11 of the Examiner's Answer contends that:

> *However, Examiner is relying on AAPA to teach wherein the amplified gradation data being gradation data at a second voltage range, as can be seen in fig. 2 of AAPA, (c) is outputted at 6v which is amplified from 3v.*

In response, paragraph [0023] of Iemoto arguably discloses that the ***flip-flop 20*** makes data input signal TM1 inputted from the counter 100, and outputs signal TM2 which held signal TM1 by the rising edge to OR gate 50 by making into a clock pulse signal the reference signal RCLK which is the constant period T.

Paragraph [0025] of Iemoto arguably discloses that ***OR gate 50*** carries out OR operation of the delay clock signal DCLK inputted as signal TM2 inputted from the flip-flop 20 from the delay circuit 32, and *outputs it to the vernier 10* as ***mix-signals TD3***.

Here, Figure 1 of Iemoto also ***fails*** to disclose, teach, or suggest the ***output of counter 100 being at 3V*** with a signal being ***input to the flip-flop 20 at 6V***, especially when there is ***no intervening circuitry*** between the output of counter 100 and the input of flip-flop 20.

As a consequence, the insertion of the level shifter 1 of AAPA between the output of counter 100 and the input of flip-flop 20 would produce a "*seemingly inoperative device*" since there is no disclosure within Iemoto of circuitry capable of processing outputs and inputs of different voltage levels.

Likewise, Figure 1 of Iemoto also ***fails*** to disclose, teach, or suggest the output of ***flip-flop 20 being at 3V*** with a signal being input to ***OR gate 50 at 6V***, especially when there is ***no intervening circuitry*** between the output of flip-flop 20 and the input of OR gate 50.

Again, the insertion of the level shifter 1 of AAPA between the output of flip-flop 20 and the input of OR gate 50 would produce a "*seemingly inoperative device*" since there is no disclosure within Iemoto of circuitry capable of processing outputs and inputs of different voltage levels.

Figure 1 of Iemoto ***fails*** to disclose, teach, or suggest the output of ***OR gate 50 being at 3V*** with a signal being input to ***vernier 10 at 6V***, especially when there is ***no intervening circuitry*** between the output of OR gate 50 and the input of vernier 10.

Accordingly, the insertion of the level shifter 1 of AAPA between the output of OR gate 50 and the input to vernier 10 would produce a "*seemingly inoperative device*" since there is no disclosure within Iemoto of circuitry capable of processing outputs and inputs of different voltage levels.

Paragraph [0026] of Iemoto arguably discloses that the ***vernier 10*** delays mix-signals TD3 inputted from OR gate 50 according to a preset value by the time resolution below the cycle T of the reference signal RCLK, and outputs it to the delay circuit 42 and the ***flip-flop 41*** as delay pulse signal TD4.

Again, Figure 1 of Iemoto ***fails*** to disclose, teach, or suggest the output of ***vernier 10 being at 3V*** with a signal being input to ***flip-flop 41 at 6V***, especially when there is ***no intervening circuitry*** between the output of vernier 10 and the input of flip-flop 41.

The insertion of the level shifter 1 of AAPA between the output of vernier 10 and the input of flip-flop 41 would produce a "*seemingly inoperative device*" since there is no disclosure within Iemoto of circuitry capable of processing outputs and inputs of different voltage levels.

Determining obviousness requires considering whether two or more pieces of prior art could be combined, or a single piece of prior art could be modified, to produce the claimed invention. *Comaper Corp. v. Antec Inc.*, 93 USPQ2d 1873, 1879 (Fed. Cir. 2010).

At least for the reasons presented hereinabove, the Examiner's Answer ***fails*** to show that AAPA and Iemoto could be combined, or that AAPA could be modified, to produce the claimed invention.

f) The combined teachings of AAPA and Iemoto *would not have* suggested the claimed invention.

Pages 11, 12 and 13 of the Examiner's Answer include the assertion that:

> *Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See In re Keller, 642 F.2d 413, 208 USPQ 871 (CCPA 1981).*

Page 12 of the Examiner's Answer includes the assertion that:

> *Iemoto is being relied upon to teach **the concept** of inserting dummy data during a quiescent period (Abstract Iemoto). AAPA, then, is being modified to include **the concept** of inserting dummy data during a quiescent period.*

Page 12 of the Examiner's Answer includes the additional assertion that:

> *Again, as noted in the preceding paragraph, examiner is not relying on Iemoto for the replacement of components, but the level shifter of AAPA as modified by **the concepts** of Iemoto.*

Page 13 of the Examiner's Answer includes the assertion that:

> *Again, as noted above, examiner is not relying on Iemoto for the replacement of components, but the level shifter of AAPA as modified by **the concepts** of Iemoto, therefore, whether or not the outputs are the same is irrelevant.*

Page 13 of the Examiner's Answer includes the additional assertion that:

> *Again, as noted in the preceding paragraphs, examiner is not relying on Iemoto for the replacement of components, but the level shifter of AAPA as modified by* ***the concepts*** *of Iemoto.*

Pages 12-13 of the Examiner's Answer include the assertion that:

> *Again, as noted in the preceding paragraphs, examiner is not relying on Iemoto for the replacement of components, but the level shifter of AAPA as modified by* ***the concepts*** *of Iemoto.*

In response to these assertions, not only does the Examiner's Answer ***fail*** to show the elements that are absent from within AAPA being disclosed within Iemoto, "*the concepts*" asserted within the Examiner's Answer are ***insufficient*** for proving obviousness of the claimed invention based upon the "combined teachings" of AAPA and Iemoto.

B. Claim 12 stands or falls alone.

Claim 12 is drawn to the display device according to claim 10, wherein said quiescent period is a horizontal blanking period.

1. Incorporation by reference

The arguments presented hereinabove with respect to claim 7 are incorporated herein by reference.

Additional arguments are provided below.

2. The Examiner's Answer *fails* to show a *horizontal blanking period* within AAPA.

Page 16 of the Examiner's Answer ***readily admits*** an ***absence*** within AAPA of a horizontal blanking period.

a) Hindsight reconstruction.

Instead, page 16 of the Examiner's Answer refers to the "Disclosure of the Invention" portion of the specification of the application for the claims on appeal.

It is impermissible, however, simply to engage in a hindsight reconstruction of the claimed invention, using the applicant's structure as a template and selecting elements from references to fill the gaps. *In re Gorman*, 18 USPQ2d 1885, 1888 (Fed. Cir. 1991).

Here, page 18 of the ***Examiner's Answer refers to Figure 5*** of the specification of the application for the claims on appeal.

However, ***Figure 5 is a timing chart used in explaining*** the correction principle shown in Figure 4, with Figure 4 being a block diagram used in explaining a correction principle for delay time according to ***the present invention***.

In this regard, the reference on page 18 of the Examiner's Answer to Figure 5 of the specification is merely a matter of *impermissible hindsight reconstruction*.

To imbue one of ordinary skill in the art with knowledge of the invention [on appeal], when no prior art reference or references of record convey or suggest that knowledge, is to fall victim to the insidious effect of a hindsight syndrome wherein that which only the inventor taught is used against its teacher. *W.L. Gore & Associates, Inc. v. Garlock, Inc.*, 220 USPQ 303, 312-313 (Fed. Cir. 1983).

b) Design choice.

Page 18 of the Examiner's Answer asserts that:

> *Therefore, Examiner asserts, while AAPA teaches a VBL [0010], whether Applicant inserts the dummy data directly into line (b), the VBL, or inserts the dummy data through line (c) (horizontal blanking period), is a matter of design choice because the function it performs is the same, namely inserting dummy data into the quiescent period.*

In response, in order for a design to be unpatentable because of obviousness, there must first be a basic design reference in the prior art, the design characteristics of which are basically the same as the claimed design. *In re Dembiczak*, 50 USPQ2d 1614, 1619 (Fed. Cir. 1999).

Regarding AAPA, there *no horizontal blanking period described within AAPA*, as confirmed on page 16 of the Examiner's Answer.

Instead, page 18 of the Examiner's Answer asserts, without providing any supporting evidence, that:

> *Examiner notes inserting dummy data during the horizontal period is not limited to horizontal blanking period but may also be inserted during the vertical blanking period.*

In response, broad conclusory statements, standing alone, are not evidence. *In re Dembiczak*, 50 USPQ2d 1614, 1617 (Fed. Cir. 1999).

Rejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness. *In re Kahn*, 78 USPQ2d 1329, 1336 (Fed. Cir. 2006).

Here, the Examiner's Answer ***fails*** to provide some articulated reasoning with some rational underpinning to support the conclusion that "*inserting dummy data during the horizontal period is not limited to horizontal blanking period but may also be inserted during the vertical blanking period*".

AAPA, while arguably disclosing vertical blanking periods, ***fails*** to disclose, teach, or suggest horizontal blanking periods.

In this regard, a finding of "obvious design choice" precluded where the claimed structure and the function it performs are different from the prior art. *In re Chu*, 36 USPQ2d 1089, 1095 (Fed. Cir. 1995).

3. The Examiner's Answer *fails* to show a *horizontal blanking period* within Iemoto.

The Examiner's Answer ***fails*** to refute arguments on page 19 of the Appeal Brief that the Final Office Action of August 20, 2009 and the Advisory Action of October 23, 2009 ***fail*** to show within Iemoto a display device wherein said quiescent period is a horizontal blanking period.

C. Claim 18 stands or falls alone.

1. Claim 18 is dependent upon claim 15.

Claim 15 is drawn to the display device according to claim 7, wherein said amplitude of the output data is changed from said second voltage range to said first voltage range, *resultant gradation data* being said output data at said first voltage range.

Claim 18 is drawn to the display device according to claim 15, wherein a horizontal driving circuit ***converts said resultant gradation data into analog signals***.

a) Incorporation by reference

The arguments presented hereinabove with respect to claim 7 are incorporated herein by reference.

Additional arguments are provided below.

b) AAPA and Iemoto, either individually or as a whole, *fail* to disclose, teach, or suggest a display device wherein a horizontal driving circuit converts said resultant gradation data into *analog signals*.

The Examiner's Answer ***fails*** to refute arguments on pages 19-20 of the Appeal Brief that AAPA and Iemoto, either individually or as a whole, ***fail*** to disclose, teach, or suggest a display device wherein a horizontal driving circuit converts said resultant gradation data into ***analog signals***.

Instead, page 19 of the Examiner's Answer contends:

> *2. Applicant asserts AAPA and Iemoto either individually or as a whole fail to disclose, teach or suggest a display device wherein a horizontal driving circuit converts said resultant gradation data into analog signals. Examiner respectfully disagrees. Gradation data applied from a horizontal driving circuit which is sequentially inputted in raster scan order to an LCD using TFTs, using a level shifter is analog data. Please see referenced Hei 10-177368 mentioned in [007] which further discusses processing of analog signals (claim 1).*

In response, the Examiner's Answer ***fails*** to show where within AAPA there is disclosed the presence of "*a horizontal driving circuit*".

Likewise, the Examiner's Answer ***fails*** to show where within Iemoto there is disclosed the presence of "*a horizontal driving circuit*".

Instead, the Examiner's Answer refers to Japanese Application Publication No. 10-177368 (Chen) for processing of analog signals.

Here, the critical inquiry is whether "there is something in the prior art as a whole *to suggest* the desirability, and thus the obviousness, of making the combination." *Fromson v. Advance Offset Plate, Inc.*, 225 USPQ 26, 31 (Fed. Cir. 1985).

In response, Chen ***fails*** to disclose, teach, or suggest a horizontal driving circuit. As a consequence, Chen ***fails*** to account for the deficiencies of AAPA and Iemoto.

But even if Chen discloses a horizontal driving circuit, the Examiner's Answer fails to show why the combination of Chen, AAPA and Iemoto would have been desirable..

ii. The Examiner erred in rejecting claim 22 as allegedly being unpatentable over AAPA and Iemoto in view of U.S. Patent No. 6,897,909 (Ochiai).

A. Claim 22 stands or falls alone.

1. Claim 22 is dependent upon claim 15.

Claim 15 is drawn to the display device according to claim 7, wherein said amplitude of the output data is changed from said second voltage range to said first voltage range, *resultant gradation data* being said output data at said first voltage range.

Claim 22 is drawn to the display device according to claim 15, wherein *an active device for processing said* ***resultant gradation data*** is formed by continuous grain silicon.

a) Incorporation by reference

The arguments presented hereinabove with respect to claim 7 are incorporated herein by reference.

Additional arguments are provided below.

b) AAPA and Iemoto, either individually or as a whole, *fail* to disclose, teach, or suggest a display device *wherein an active device for processing said resultant gradation data is formed by continuous grain silicon.*

Page 8 of the Examiner's Answer readily admits that AAPA and Iemoto, either individually or as a whole, ***fail*** to disclose, teach, or suggest a display device *wherein an active device for processing said resultant gradation data is formed by continuous grain silicon.*

c) The Examiner's Answer *fails* to show that the skilled artisan would have combined AAPA and Iemoto with Ochiai.

Ochiai arguably discloses that the term "polysilicon" also encompasses macrocrystalline silicon and ***continuous grain silicon (CGS)*** as well as single-crystal silicon (Ochiai at column 23, lines 48-50).

However, the Examiner's Answer ***fails*** to show Ochiai as providing for each and every feature that has been shown to be deficient from within AAPA and Iemoto.

Conclusion

The prior art of record fails to disclose, teach or suggest all the features of the claimed invention.

For the foregoing reasons, all the claims now pending in the present application are allowable, and the present application is in condition for allowance.

For at least the reasons set forth hereinabove, the rejection of the claimed invention should not be sustained.

Therefore, a reversal of the rejection is respectfully requested.

If any additional fee is required or any overpayment made, the Commissioner is hereby authorized to charge the fee or credit the overpayment to Deposit Account # 18-0013.

Dated: May 28, 2010

Respectfully submitted,

By _____
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